Driving SiC to its Limit:

Reviewing Advances in SiC MOSFET Technology that will Reduce EV Converter Costs

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29th February 2024

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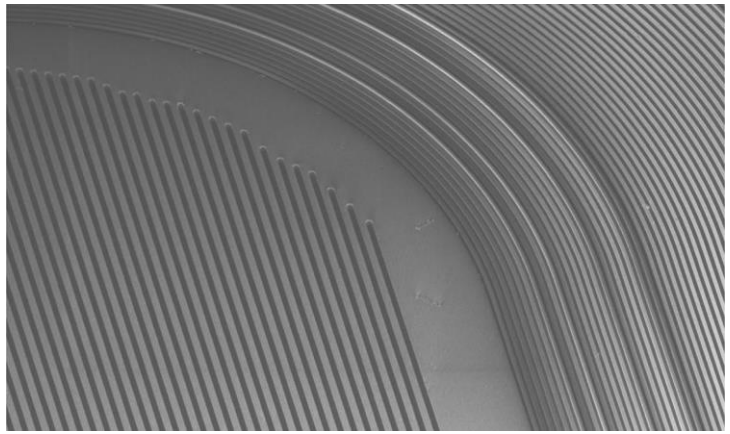

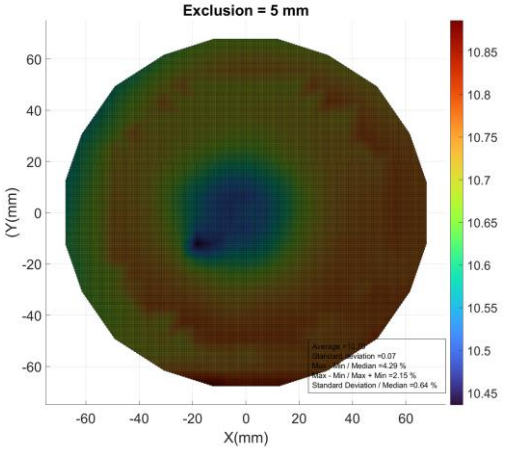

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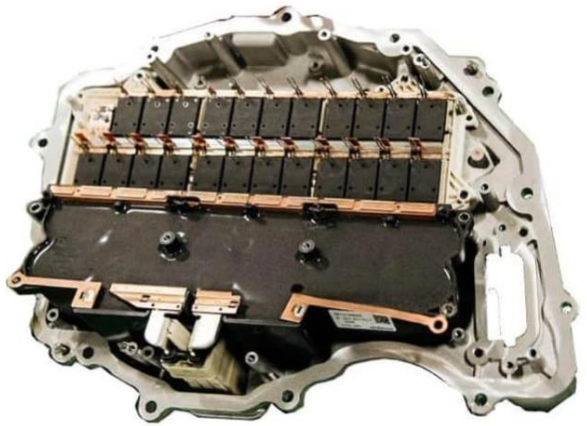

Peter Gammon
Mar 16, 2023 · 9 min

Examining Tesla's 75% SiC Reduction

In 2017, Tesla broke new ground by developing a silicon carbide (SiC) drivetrain inverter for their Model 3, becoming the first electric...

7,560 views 1 comment 8

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Contents

- **Introduction - Silicon Carbide Cost Drivers**
- SiC MOSFET Modelling
- Reducing a MOSFET's Channel and Substrate Resistances
- Reducing a MOSFET's Drift Resistance
- Combined $R_{ON,SP}$ Reduction Model
- Conclusion

Silicon Carbide Cost Drivers

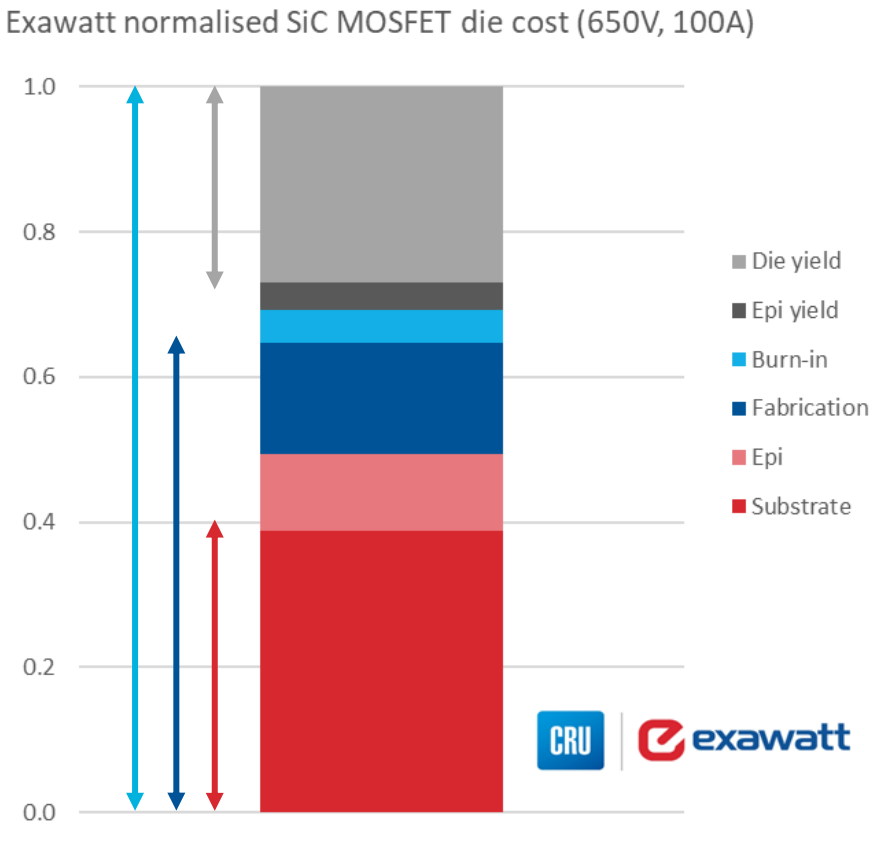
Costs of SiC power devices are rapidly falling driven by a fast-expanding market

Incremental yield improvements:

- 200mm fabs
- Improved gate designs
- Defect density

Expanding Industry

- Multi $bn expansion
- New entrants
- Expanding supply chain
- Vertical integration
- The rise of China



With thanks to Adam Dawson and Bex Stone at Exawatt - exa-watt.com/power-electronics/ for more information

Die size reduction
Generational device improvement

Large area substrates:

- 200 mm wafers
- Yield improvement

Wafering and reuse

- Laser dicing methods
- Wafer splitting
- N times reuse

The currency of die size reduction is specific on-resistance - $R_{ON,SP}$

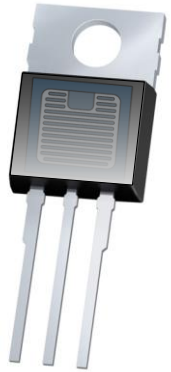
The currency of die size reduction is specific on-resistance:

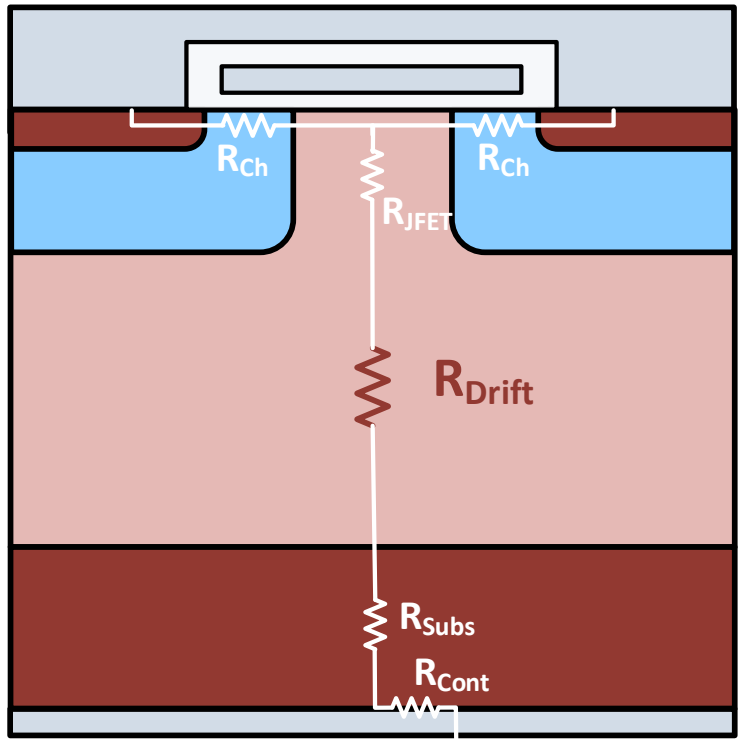
$$R_{ON,SP} = A_{Active} \times R_{ON}$$

A_{Active} is the die area minus the termination and gate pad areas.

$$R_{ON} = R_{Drift} + R_{Ch} + R_{JFET} + R_{Subs} + R_{Other}$$

Lower the $R_{ON,SP}$ components and die size is reduced for given product





SiC MOSFETs a history in $R_{ON,SP}$

CREE

CPMF-1200-S080B

Z-FET™ Silicon Carbide MOSFET

N-Channel Enhancement Mode

Bare Die

V_{DS}	= 1200 V
$R_{DS(on)}$	= 80 mΩ
Q_g	= 90.8 nC

(One of) the first 1200V SiC MOSFETs, released by Cree in 2011

life.augmented

SCTW100N65G2AG

Datasheet

Automotive-grade silicon carbide Power MOSFET 650 V, 100 A, 20 mΩ (typ., T_J=25 °C), in an HiP247™ package

(One of) the first 650V SiC MOSFETs, released by ST in 2016

ROHM SEMICONDUCTOR

SCT4013DR

N-channel SiC power MOSFET

Datasheet

V_{DSS}	750V
$R_{DS(on)}$ (Typ.)	13mΩ
I_D *1	105A
P_D	312W

●Outline

TO-247-4L

The current lowest $R_{ON,SP}$: 750V SiC MOSFETs, released by Rohm in 2022

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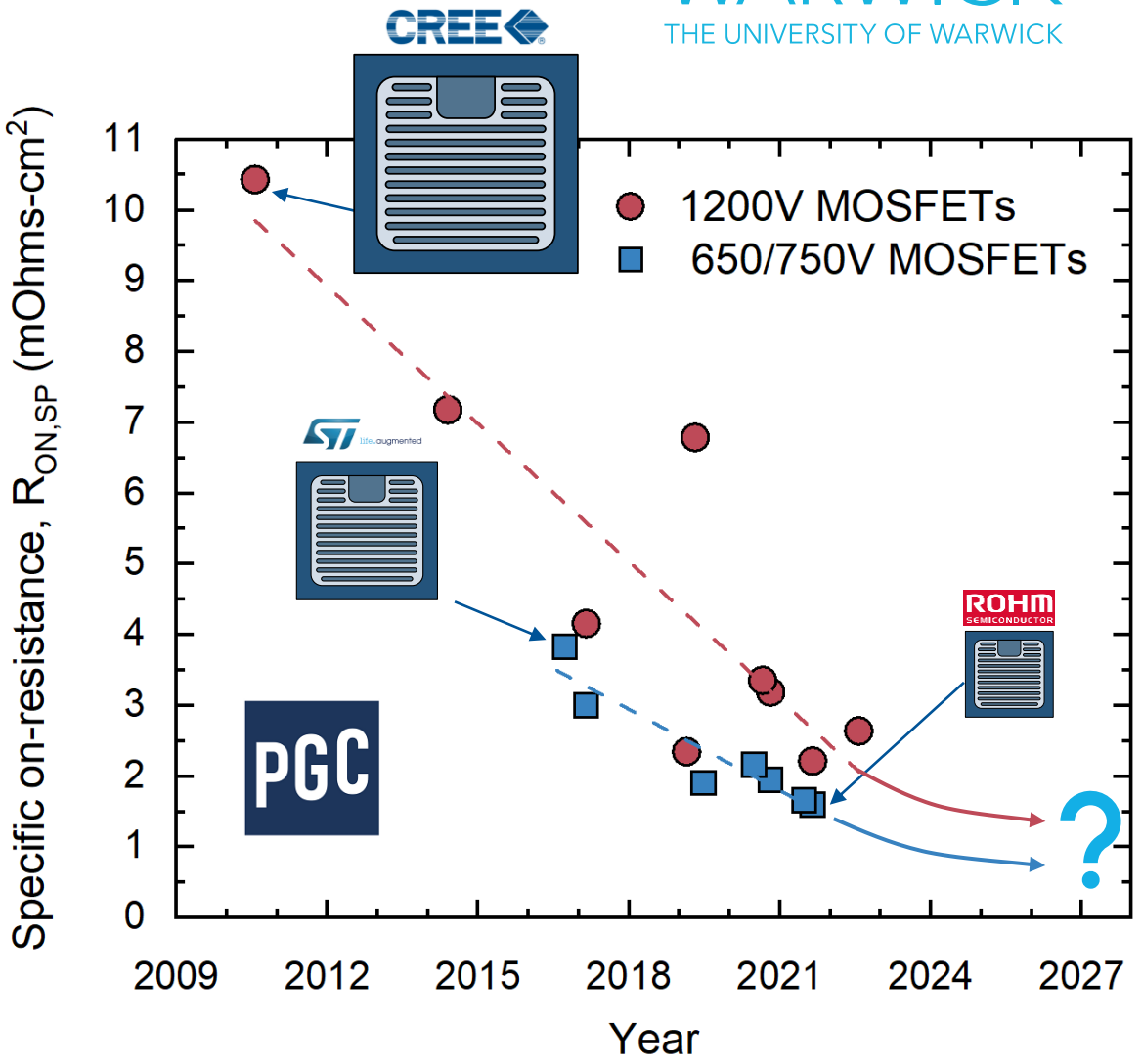


$R_{ON,SP}$ driving cost reduction

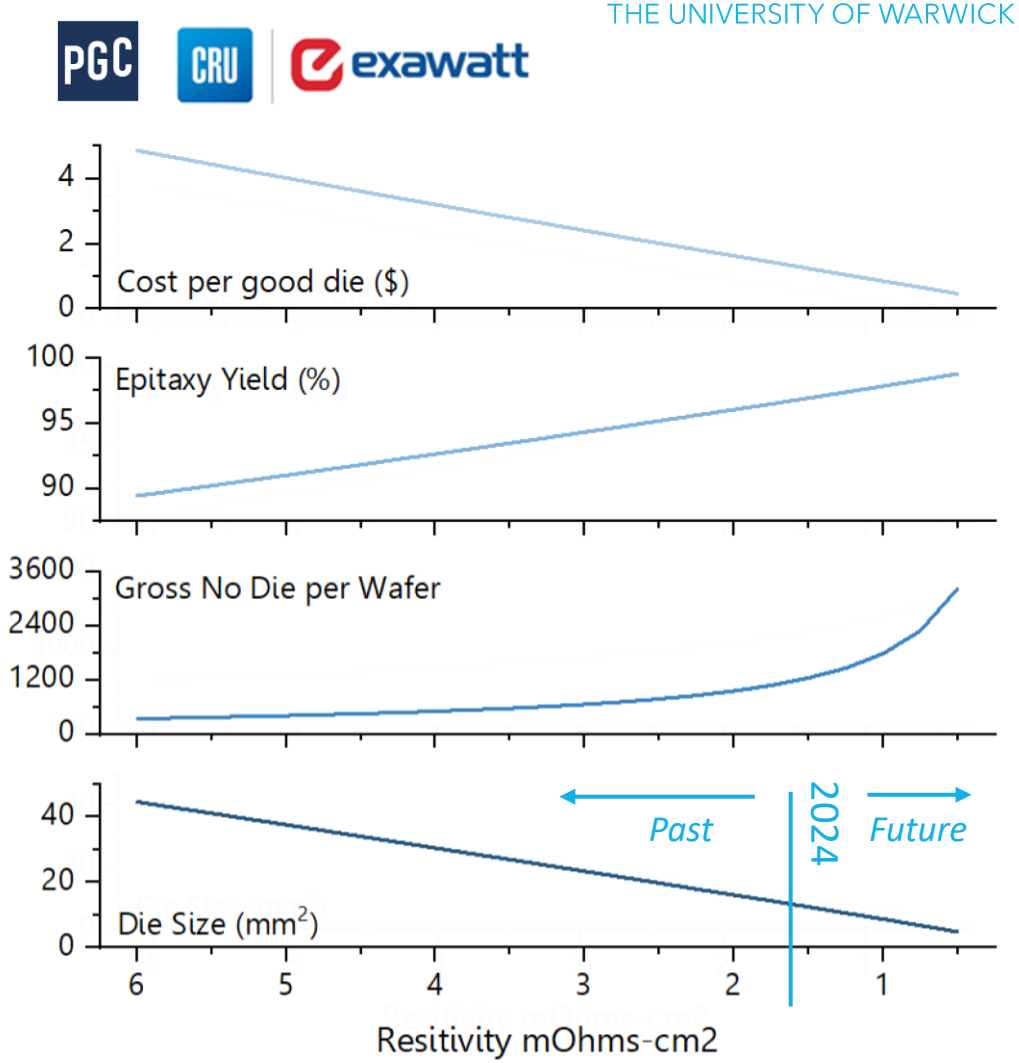
The currency of die size reduction is specific on-resistance:

$$R_{ON,SP} = A_{Active} \times R_{ON}$$

As $R_{ON,SP}$ reduces:

- Dies sizes reduce for a given R_{ON} (15 mΩ)
- More die are produced per wafer
- Fewer die (as a % of wafer) killed by defects
- Cost of good die reduces

Lower $R_{ON,SP}$ = Higher Yields = Lower costs



Model is a fictional scenario in which die of Ron=15mOhm, are produced on a 150mm substrate with a defect density of 0.25cm^{-2}, with a $1500 wafer processing cost

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Modelling Rohm's Low $R_{ON,SP}$ MOSFETs

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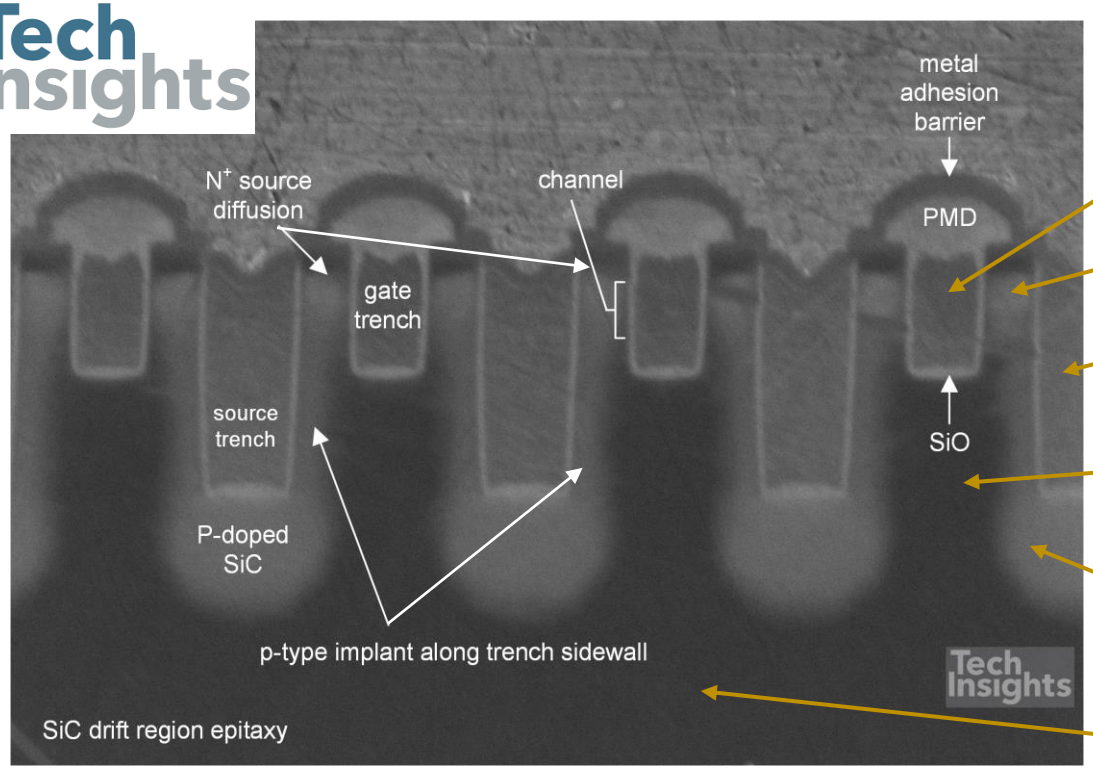
Focussing on Rohm's 4th Gen 750V MOSFET: the device with today's lowest $R_{ON,SP}$.



Rohm's Trench 750 V SCT4045DE

Recessed Gate Trench

Vertical channel

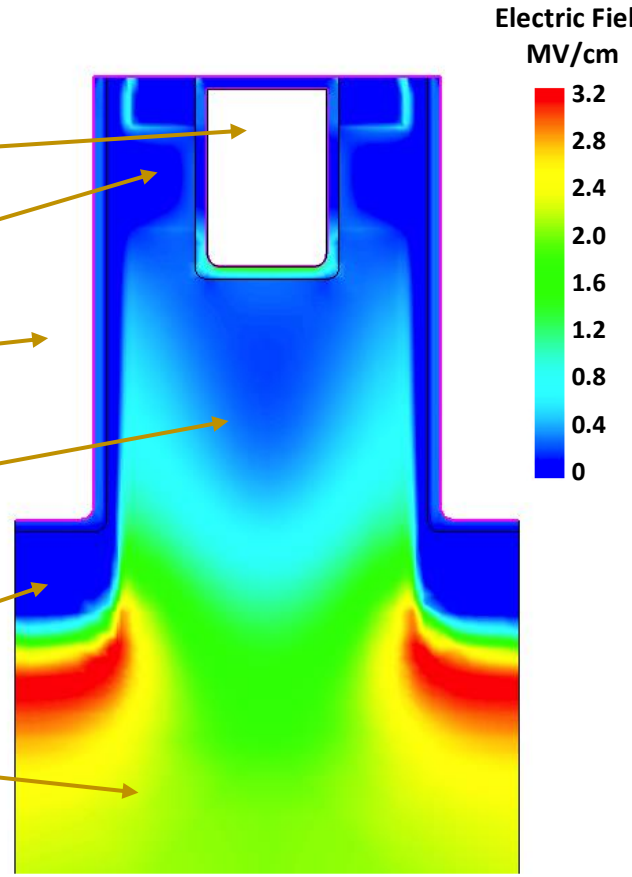
Deep Source Trenches

JFET region that saturates in off state

P-implant to sink the electric field peak

N-type drift region

(Thinned Substrate)

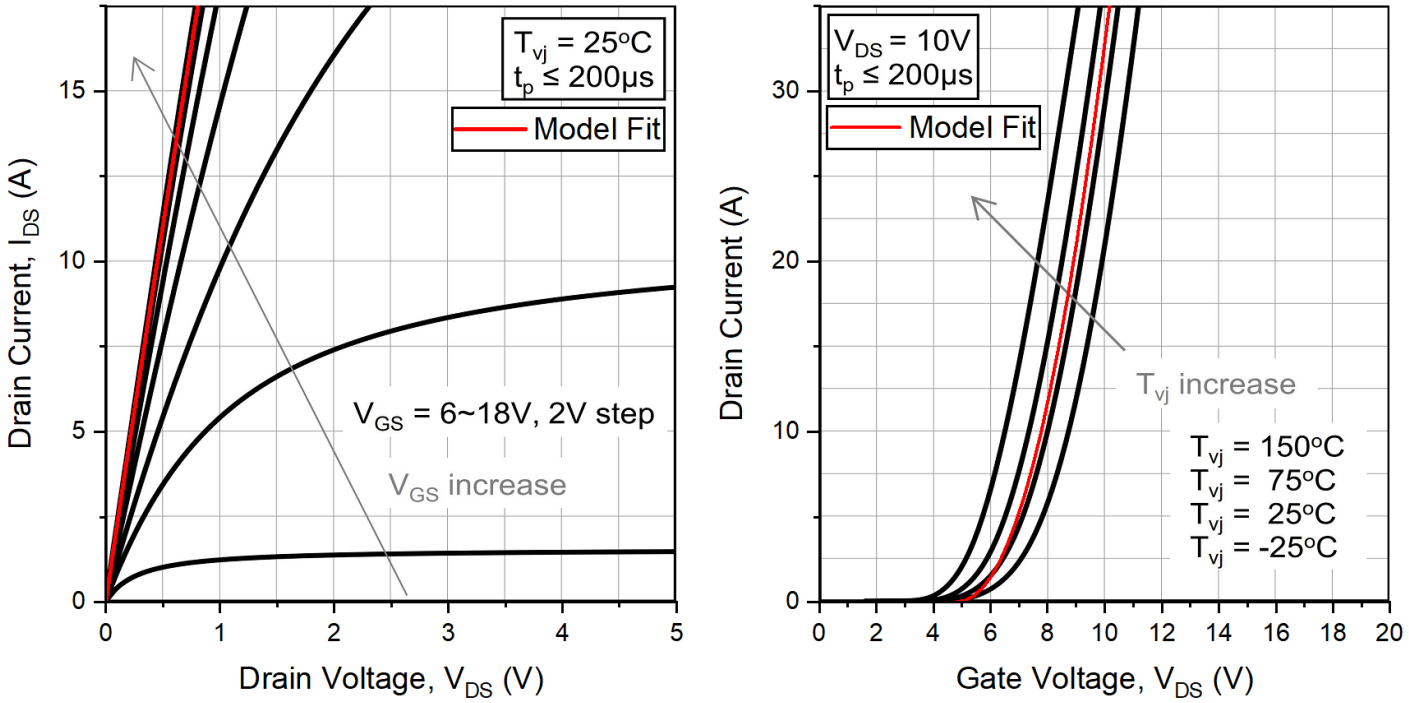


TCAD Simulation, structure and off-state

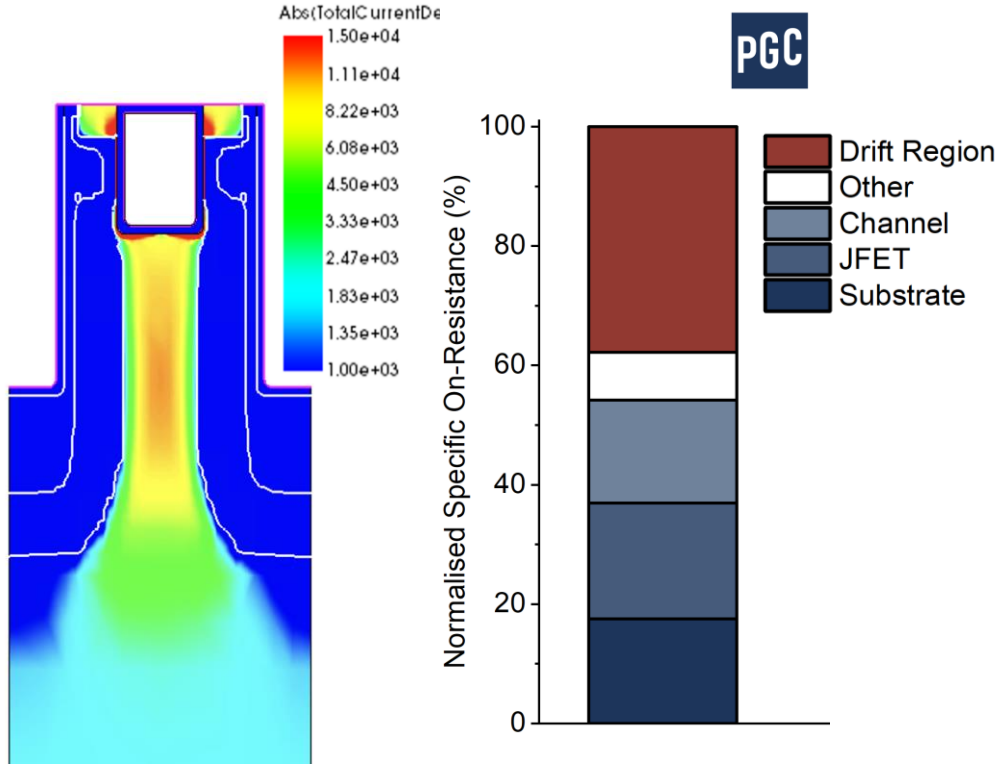
With thanks to Steve Russell at TechInsights - srussell@techinsights.com for more information

Modelling Rohm's Low $R_{ON,SP}$ MOSFETs

Varying doping regions, trap profiles, contact resistivities and other features resulted in adequate datasheet fitting.



Datasheet images from 750V Rohm SCT4045DE with Warwick TCAD overlayed



Current density, and resistance components taken from Warwick's TCAD models

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Reducing $R_{ON,SP}$: Substrate Resistance

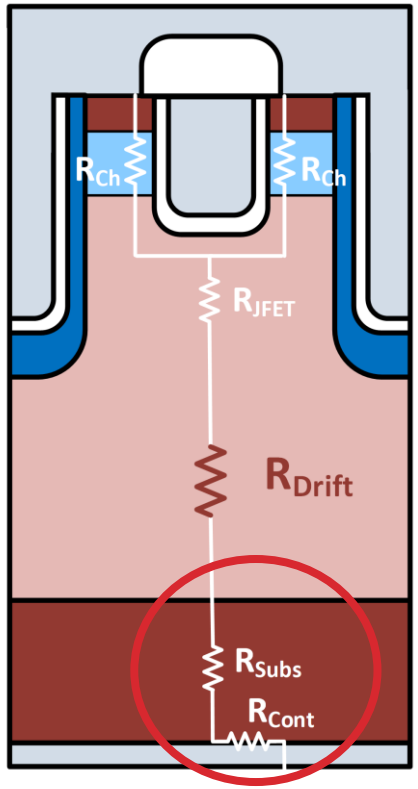
R_{subs} accounted for 17% of the Warwick Trench MOSFET model.

Issues at the technology limit:

- During boule growth increasing dopant density too far increases defect density. N_D is typically ≤1e19 cm^{-3}.
- This leads to large R_{subs} and back contact resistance!
- Substrates cut to 350 µm to ensure robustness during handling.

Current state of the art processing methods include:

- Back grinding to ~100-180µm
- Laser annealing of back contact



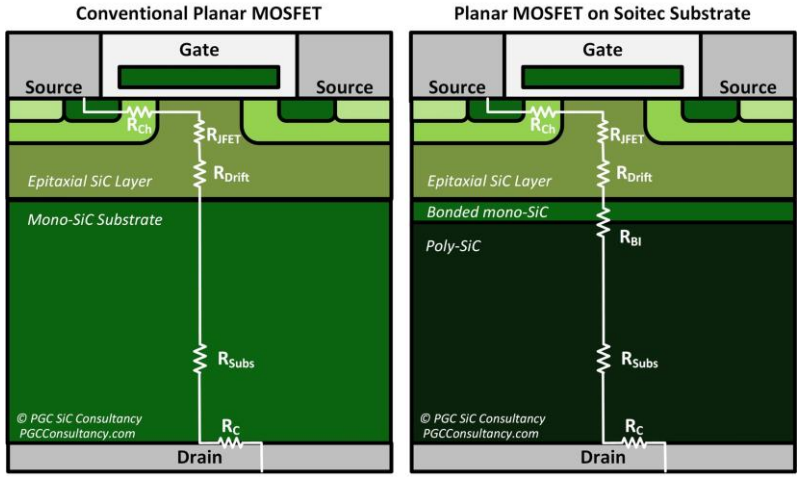
Reducing $R_{ON,SP}$: Substrate Resistance

Engineered Substrates: Soitec and SICOXS

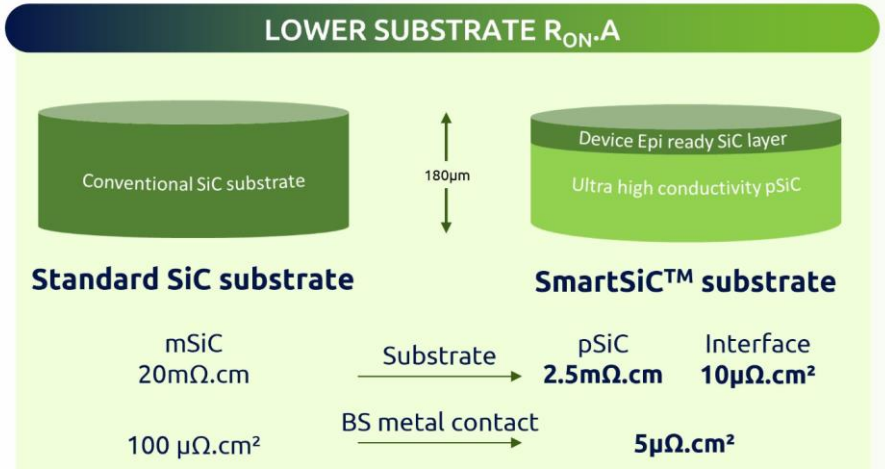
A wafer bonding and wafer splitting process is used to transfer a thin mono-SiC layer onto a low resistance poly-SiC substrate.

PolySiC doping >> MonoSiC doping resulting in:

- Much reduced $R_{subs,Sp}$. Up to 8x lower (per Soitec)
- Very low contact resistance – possibly even without the need for laser annealing.



PGC Article: *A deep dive into Soitec's SiC Substrates*, available: www.pgcconsultancy.com/post/rohm-gen-4-a-technical-review



Source: Soitec

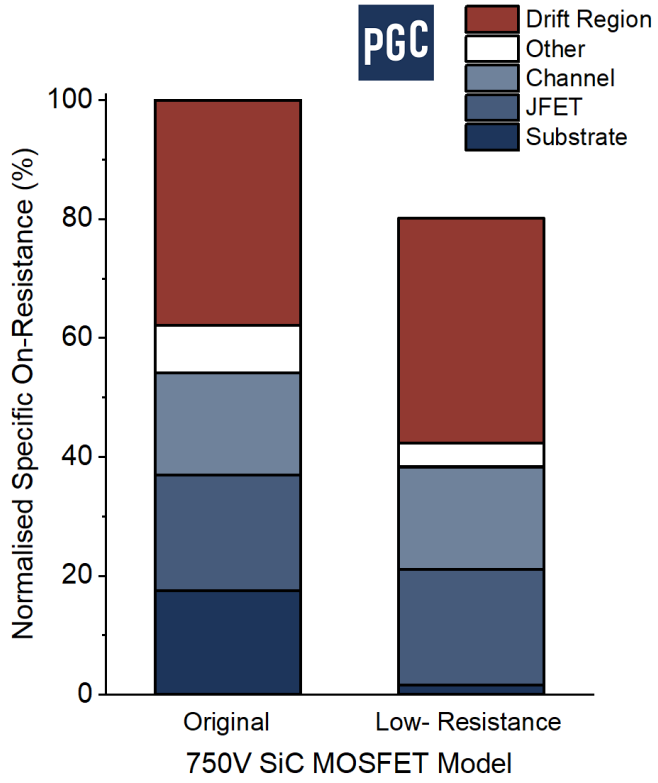
Reducing $R_{ON,SP}$: Substrate Resistance

Modelling Substrate Resistance reduction

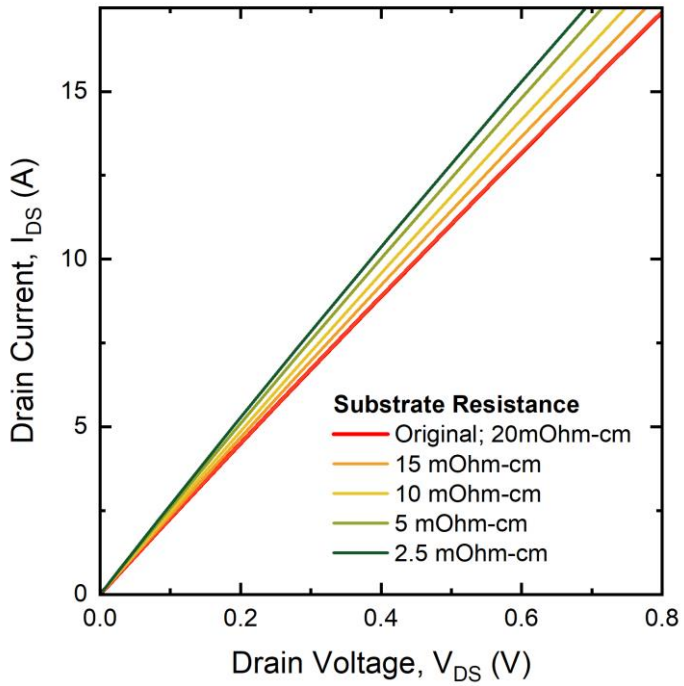
Starting from the Warwick model substrate resistance is lowered by increasing $N_{D,subs}$, and contact resistivity is reduced from 10^{-4} Ω.cm² to 10^{-5} Ω.cm².

When R_{Subs}=2.5 mOhm:

- $R_{ON,SP}$ reduced by 19%.
- Active area reduced by 9%



Up to -19% R_{onsp}
→ -9% A_{Active}



Reducing $R_{ON,SP}$: Channel Resistance

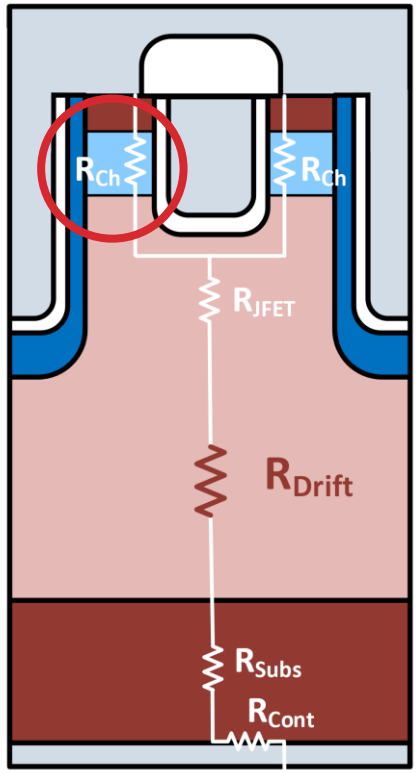
R_{Chan} ≈ 17% of the Warwick Trench MOSFET model.

Issues at the technology limit:

- Imperfect thermal oxidation; charge trapped in the oxide and the interface; reduced channel mobility.
- Alternative oxidation “solutions” often worse than the “cure”, when reliability considered.

Current state of the art processing methods include:

- Post oxide anneals in NO/N_2O; mobilities of ~15-25 $cm^2/V.s$
- Narrow channel regions, thinner oxides, trench designs and reduced cell pitches can provide compensation.



Reducing $R_{ON,SP}$: Channel Resistance

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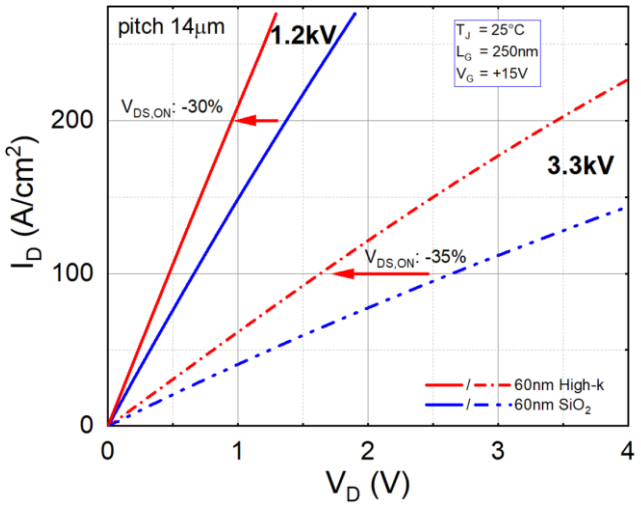
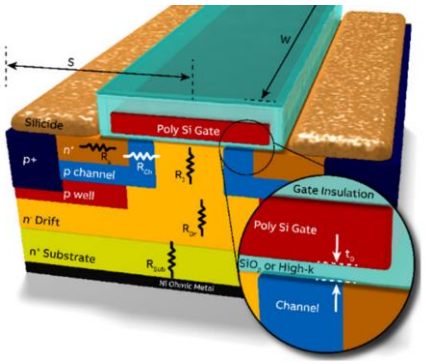
ALD based High-K dielectrics

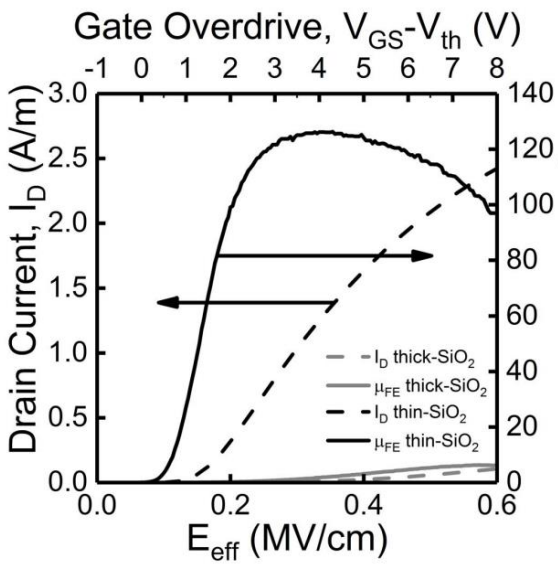
Hitachi Energy [1]: “High-K” stacks with low D_{IT}, 1000 yr TDDB reliability and minimal V_{TH} drift.

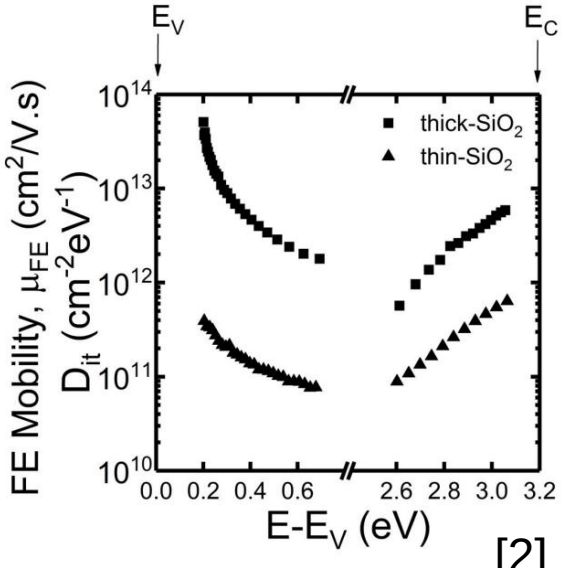
Newcastle University [2] and Wolfspeed [3] have achieved mobilities beyond 100 $cm^2/V.s$ using Al_2O_3 – without needing nitridation anneals





[1]





[2]

[1] Wirths *et al*., High-k dielectrics for SiC power MOSFET technology: unrivaled reliability, ruggedness and performance, Hitachi Energy
[2] F. Arith *et al*., IEEE Electron Device Letters, vol. 39, no. 4, pp. 564, 2018
[3] D. J. Lichtenwalner *et al*., *Appl. Phys. Lett.*, vol. 95, pp. 152113, 2009.

Reducing $R_{ON,SP}$: Channel Resistance

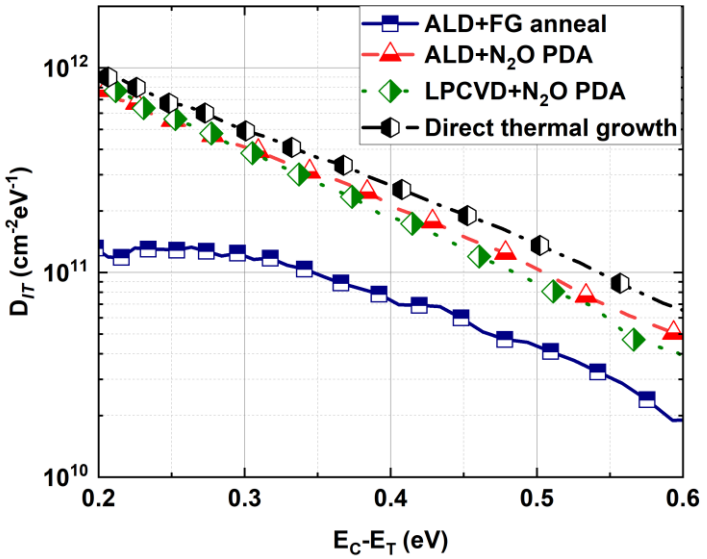
ALD based SiO_2 deposition

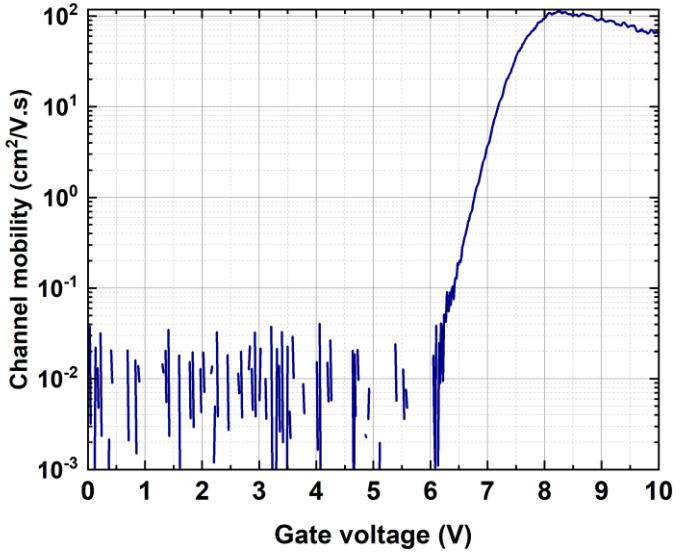
A SiO_2 ALD Oxide process has been developed at Warwick

A forming gas anneal results in a Si-rich interface.

Low D_{IT} densities of 10^{11}-10^{12} cm^2/eV result in mobilities of 60 $cm^2/V.s$ at room temperature,100 $cm^2/V.s$ at 175°C.

Robust TDDB measurements prove process could transfer to commercial devices





[1] Renz et al. *ECS Transactions*, *108 (*2), p.43, 2022

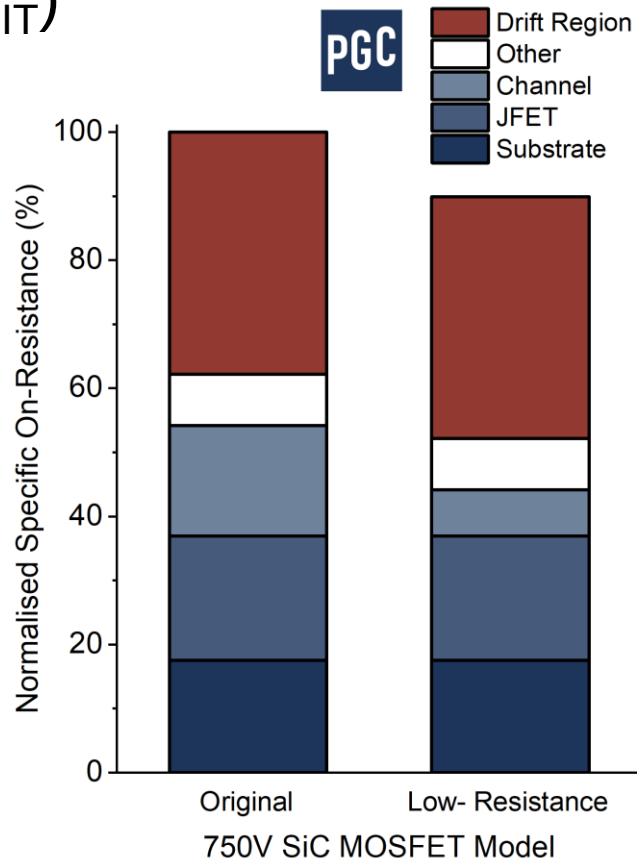
Reducing $R_{ON,SP}$: Channel Resistance

Modelling Channel Resistance reduction

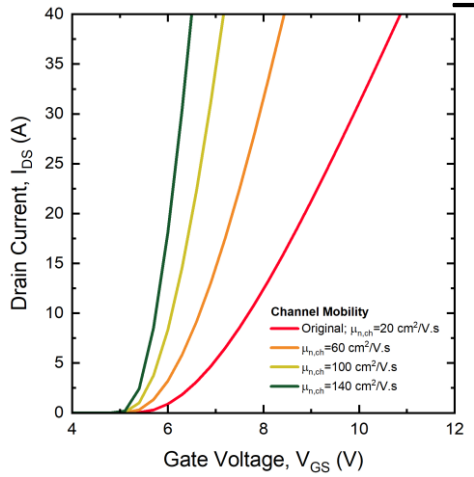
In the Warwick model, channel mobility is increased by lowering interfacial trap densities (D_{IT})

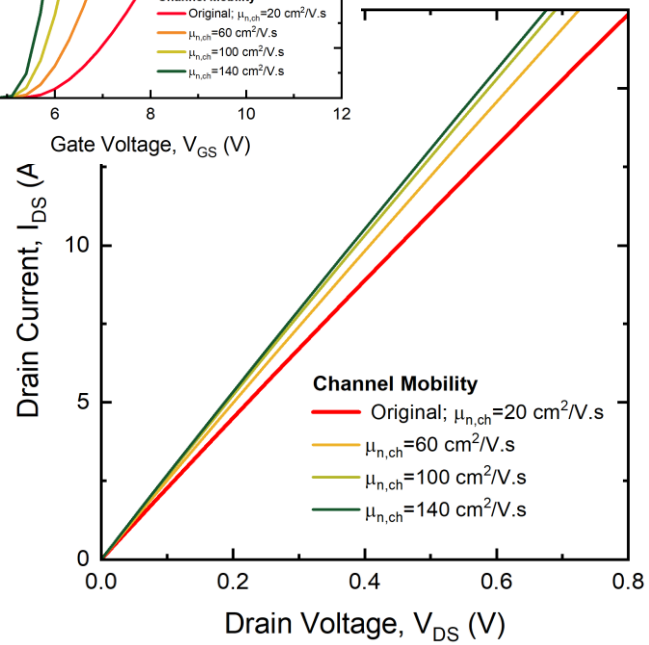
Reducing the traps to achieve μ_{Ch}=60 cm²/V.s resulted in:

- 58% reduction in R_{Ch}
- 10.3% $R_{ON,SP}$ reduction and 5% die active area reduction
- 85% increase in dI_{DS}/ dV_{GS}



Up to -10% R_{onsp}
→ -5% A_{Active}





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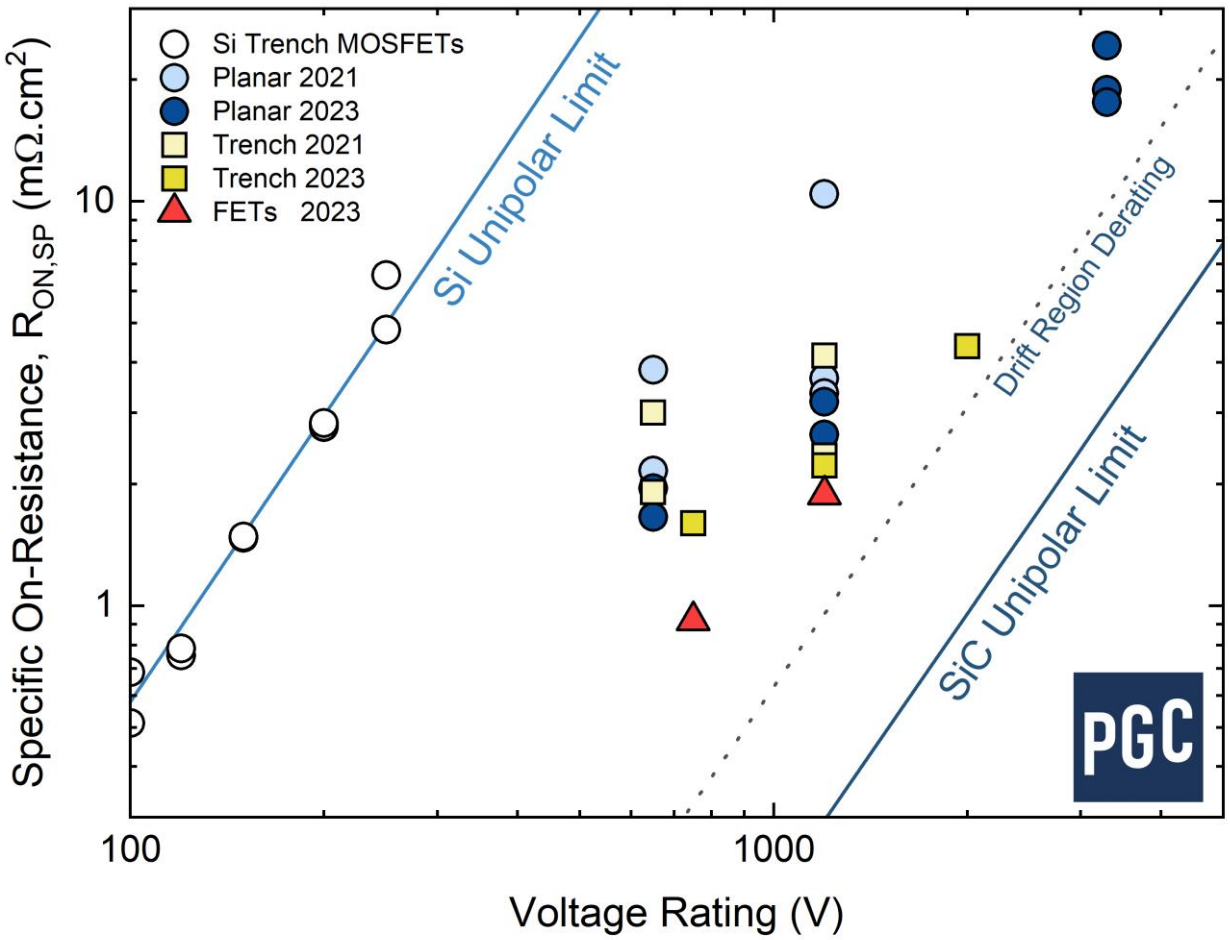
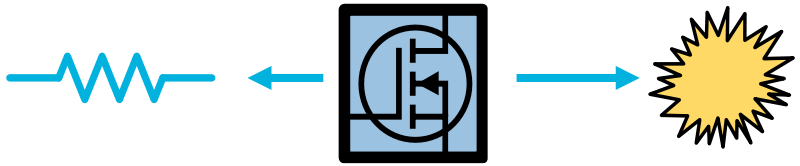
Drift Region Optimisation

Textbook drift region optimisation considers only the breakdown voltage vs on resistance, leading to the unipolar limit.





To optimise **Breakdown voltage**:

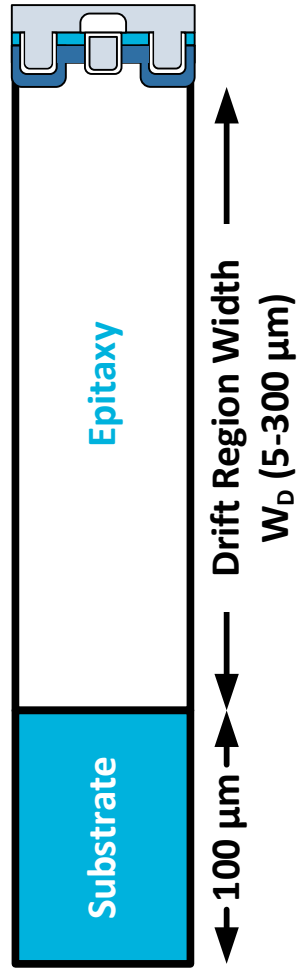
$$V_{BD} = W_D\left(E_{max,Si} - W_D\frac{qN_D}{2\varepsilon_s}\right)$$

Maximise W_D

To optimise **On-Resistance**:

$$R_{Dr} \cong \frac{W_D}{AqN_D\mu_n}$$

Minimise W_D



Explaining SiC drift region derating

“Derating” involves designing the device to breakdown a margin above the rated voltage.

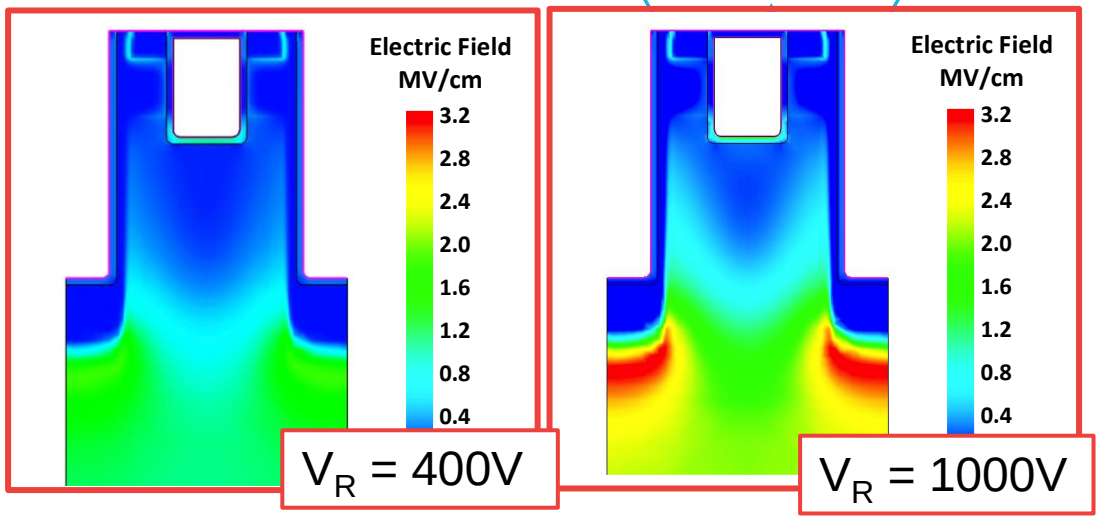
This reduces the electric field present around the gate oxide.

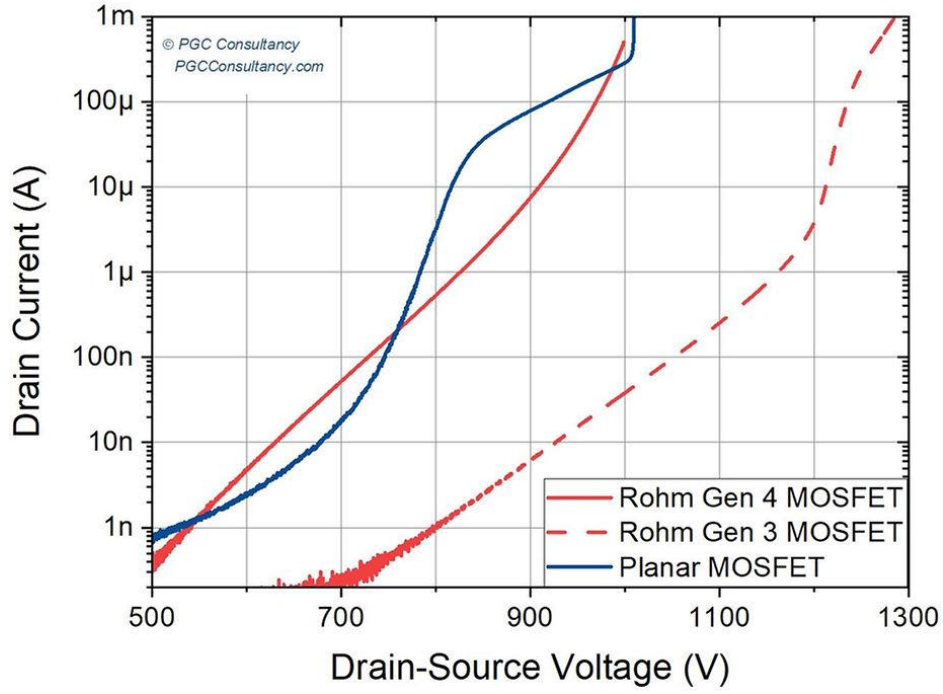
In our simulations:

- E-field in oxide at 1000V = 1.1 MV/cm
- E-field in oxide at 400V = 0.9 MV/cm

This protects the gate from stress, improving:

- Short circuit withstand time
- Immunity to SEGR during cosmic ray strike





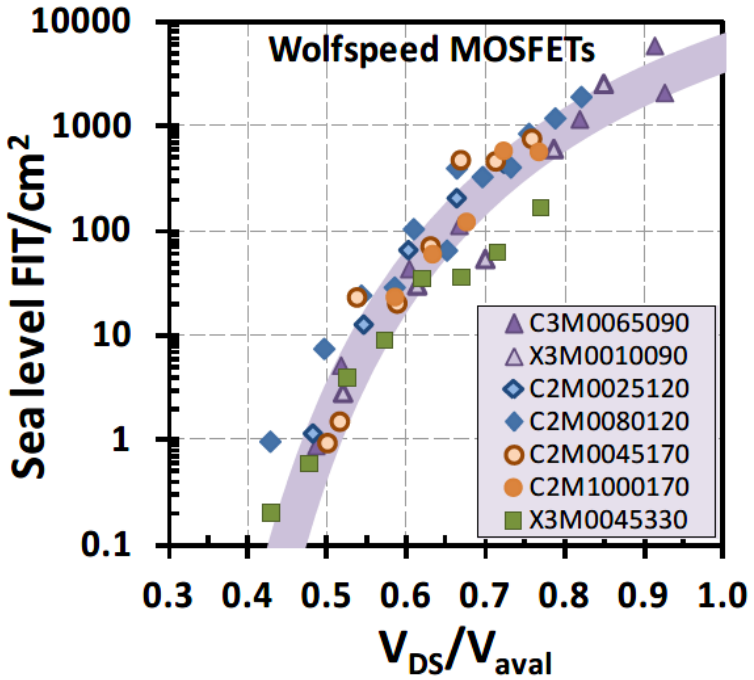
Explaining SiC drift region derating

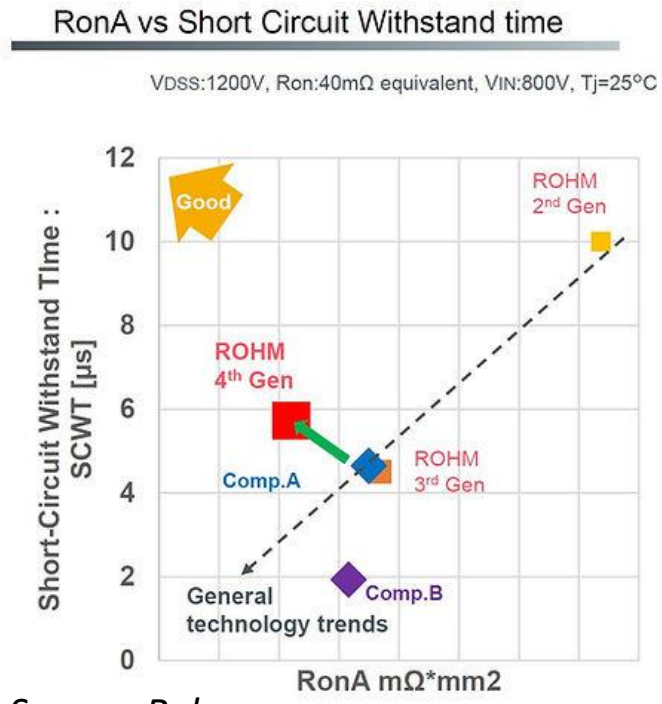
An over designed drift region provides short circuit immunity.

For cosmic ray immunity, an automotive FIT rate [2] of 0.1 FIT/cm^2, requires a V_{DS}/V_{aval} of 0.4 [1].

i.e. for a 650V MOSFET to be used in a 400V system: V_{aval} = 1000V.

FIT rates of SiC MOSFETs from Wolfspeed display a universal scaling behaviour [1].





Source: Rohm

[1] D. J. Lichtenwalner et al. "Materials Science Forum. Vol. 924 pp 559, 2018.
[2] JEDEC Standard JEP151A, available: www.jedec.org/standards-documents/docs/jep151

Reducing $R_{ON,SP}$: Substrate Resistance

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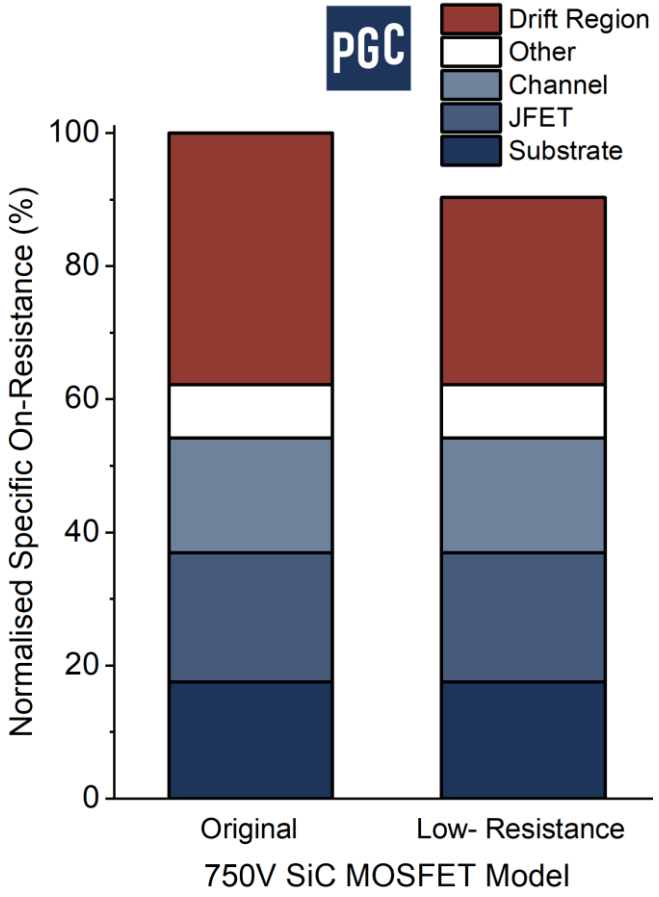
Modelling Drift Resistance reduction

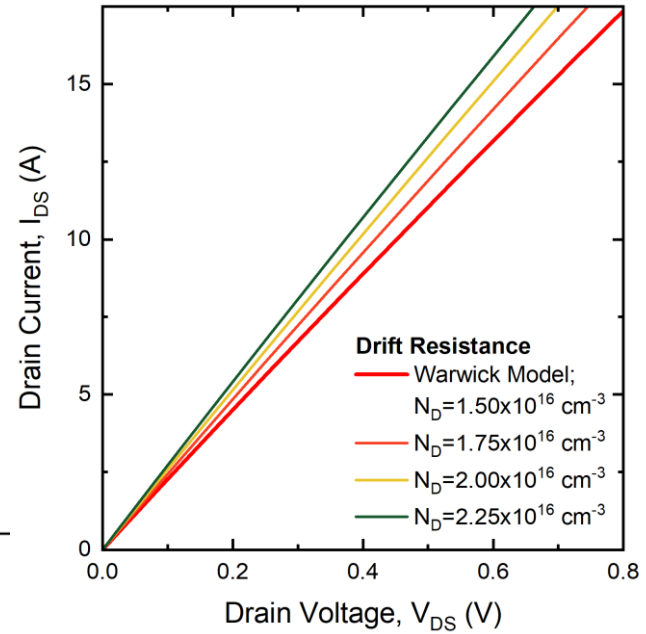
In the Warwick model, drift resistance is lowered by incrementally increasing N_{Drift}

Increasing N_{Drift} by 33% resulted in:

- 25% reduction in R_{Dr}
- 9.6% $R_{ON,SP}$ reduction and 6% die active area reduction
- **But**: 15% reduction in V_{BD} to 875V.
- Oxide E-field increased 10% to 1.33 MV/cm
- Reduced cosmic ray immunity

Up to -9.6% R_{onsp}
→ -4.9% A_{Active}





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Contents

- Introduction - Silicon Carbide Cost Drivers
- SiC MOSFET Modelling
- Reducing a MOSFET's Channel and Substrate Resistances
- Reducing a MOSFET's Drift Resistance
- **Combined $R_{ON,SP}$ Reduction Model**
- Conclusion

Reducing $R_{ON,SP}$: A combined low-resistance model

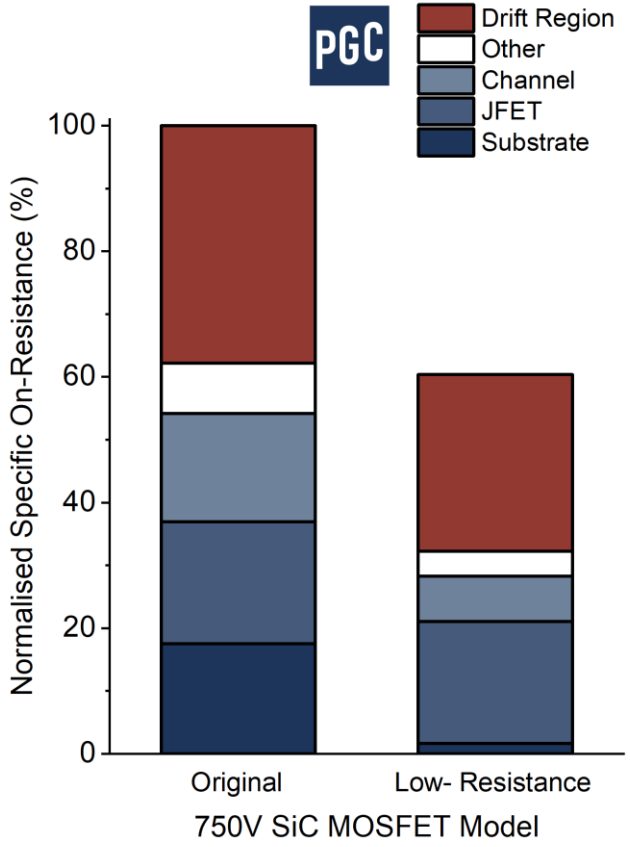
Starting with our original models, we produced a combined low resistance version including:

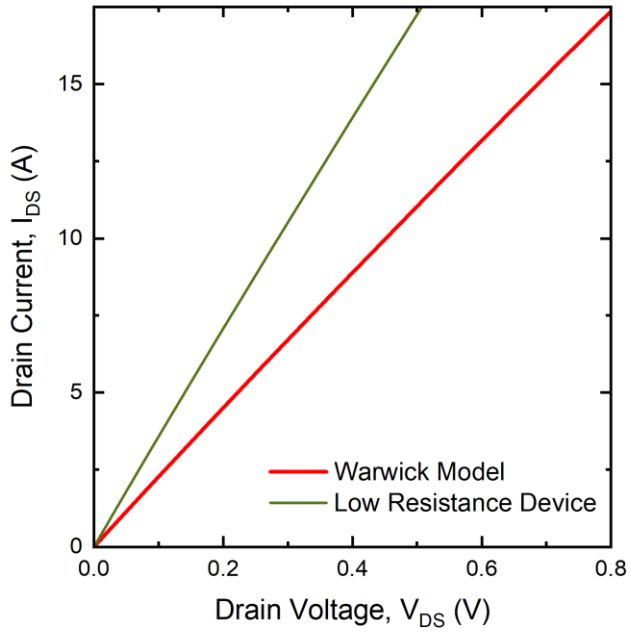
- 33% higher N_{drift}.
- 8x lower substrate resistivity
- Channel mobility = μ_{Ch}=60 $cm^2/V.s$

Resulting in:

- 40% $R_{ON,SP}$ reduction and 23% die active area reduction
- A V_{BD} of 875V.

Up to -40% R_{onsp}
→ -23% A_{Active}



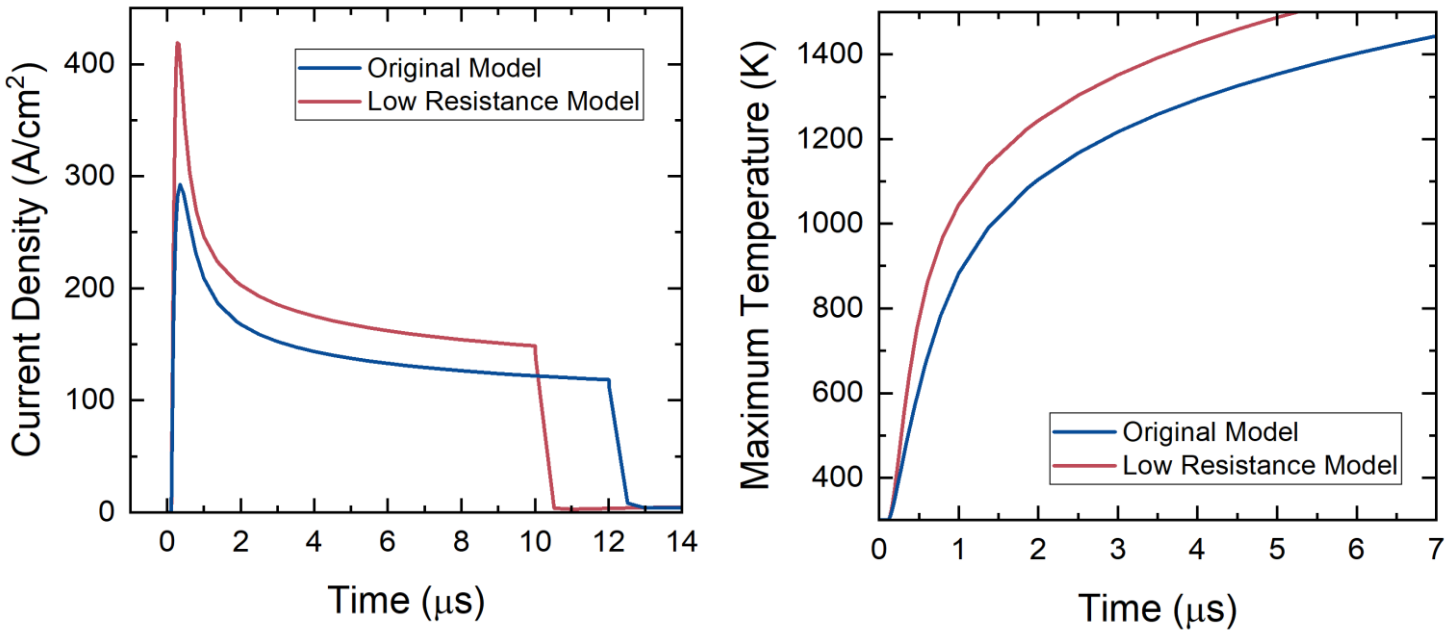


Paying the price of $R_{ON,SP}$ reduction

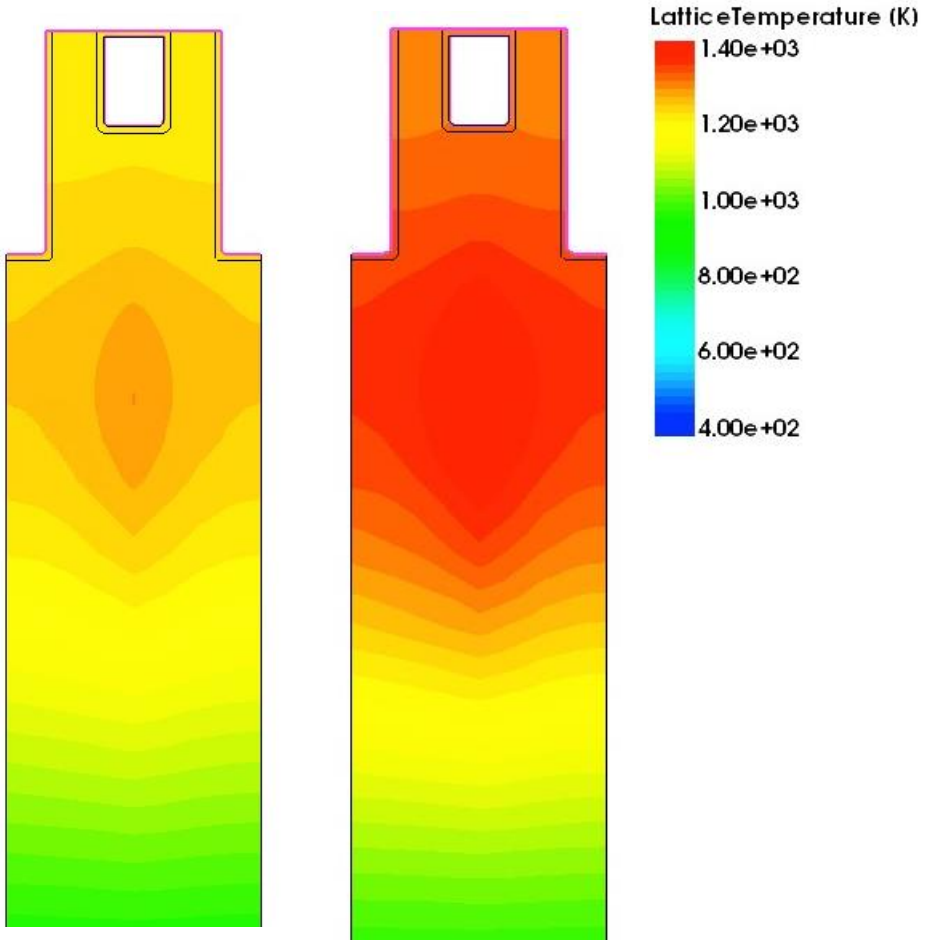
Resistance reduction does not come for free.

Last pass short circuit simulations reveal:

- An increased current peak (300 to 400 A/cm^2)



Short circuit simulations carried out on the original and low resistance MOSFETs using V_{DS}=400V, R_G= 10Ω



Temperature profiles of the original and low-resistance 750V MOSFETs after 4μs of short circuit exposure

Conclusion

- Cost reduction continues to be driven by many factors in the maturing SiC MOSFET market
- New releases of low $R_{ON,SP}$ devices result in cost step changes.
- In the coming drive to trench, innovation in the substrate, and the channel could drive further reductions in $R_{ON,SP}$.
- Reducing the drift region resistance is possible but relies on optimal gate oxide protection to protect it from high electric fields.
- All $R_{ON,SP}$ reductions increase current density in fault conditions, and therefore reliability and robustness will trade off with resistance reduction.